In the Claims:

1-14. (Cancelled)

15. (Withdrawn)

16. (Currently Amended) A semiconductor package, comprising:

a leadframe having:

a chip paddle defining opposed top and bottom surfaces and a plurality of sides and corners; and

a plurality of leads extending along at least one of the sides of the chip paddle in spaced relation thereto, each of the leads defining opposed top and bottom surfaces**, the bottom surfaces of the leads being of at least two difference lengths**;

a semiconductor chip mounted to the top surface of the chip paddle and electrically connected to at least one of the leads; and

an encapsulation material covering the leadframe and the semiconductor chip such that the bottom surfaces of the leads**, which are of at least two different lengths,** are exposed in the encapsulation material~~;~~

~~the leads being configured such that the bottom surfaces thereof which are exposed in the encapsulation material are of at least two different lengths~~.

17. (Previously Added) The semiconductor package of Claim 16 wherein the leads are segregated into multiple sets which extend long respective ones of the sides of the chip paddle in spaced relation thereto.

18. (Previously Added) The semiconductor package of Claim 17 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surfaces of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

19. (Previously Added) The semiconductor package of Claim 18 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

20. (Previously Added) The semiconductor package of Claim 18 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

21. (Previously Added) The semiconductor package of Claim 16 wherein the bottom surface of the chip paddle is exposed in the encapsulation material.

22. (Previously Added) The semiconductor package of Claim 21 wherein:

the encapsulation material defines a generally planar bottom surface;

the bottom surface of the chip paddle is generally planar and substantially flush with the bottom surface of the encapsulation material; and

the bottom surfaces of the leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

23. (Previously Added) The semiconductor package of Claim 16 wherein the leadframe further comprises at least one tie bar attached to and extending from at least one of the corners of the chip paddle, the tie bar defining opposed top and bottom surfaces.

24. (Previously Added) The semiconductor package of Claim 23 wherein the bottom surface of the at least one tie bar is exposed in the encapsulation material.

25. (Currently Amended) A semiconductor package comprising:

a plurality of leads, each of the leads defining opposed top and bottom surfaces**, the bottom surfaces of the leads being of at least two different lengths**;

a semiconductor chip defining multiple sides and electrically connected to at least one of the leads; and

an encapsulation material covering the leads and the semiconductor chip such that the bottom surfaces of the leads**, which are of at least two different lengths,** are exposed in the encapsulation material~~;~~

~~the leads being configured such that the bottom surfaces thereof which are exposed in the encapsulation material are of at least two different lengths~~.

26. (Previously Added) The semiconductor package of Claim 25 wherein the leads are segregated into multiple sets which extend along respective ones of the sides of the semiconductor chip.

27. (Previously Added) The semiconductor package of Claim 26 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surface of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

28. (Previously Added) The semiconductor package of Claim 27 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

29. (Previously Added) The semiconductor package of Claim 27 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

30. (Previously Added) The semiconductor package of Claim 25 wherein:

the encapsulation material defines a generally planar bottom surface; and

the bottom surfaces of the leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

31. (Previously Added) In a semiconductor package comprising a plurality of leads having bottom surfaces which are exposed in an encapsulation material and a semiconductor chip which is covered by the encapsulation material and electrically connected to at least one of the leads, the improvement comprising:

configuring the leads such that the bottom surfaces thereof which are exposed in the encapsulation material are of at least two different lengths.

32. (Previously Added) The semiconductor package of Claim 31 wherein the semiconductor chip defines multiple sides, and the leads are segregated into multiple sets which extend along respective ones of the sides of the semiconductor chip.

33. (Previously Added) The semiconductor package of Claim 32 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surfaces of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

34. (Previously Added) The semiconductor package of Claim 33 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

35. (Previously Added) The semiconductor package of Claim 33 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.